

IN THE SPECIFICATION:

Page 5, lines 3-9:

-- In accordance with preferred embodiments of the present invention, a data processor preferably includes a central processing unit ("CPU") and an address translation unit ("ATU") that preferably receives a virtual addresses output from the central processing unit and outputs a physical address, wherein the address translation unit preferably includes a first translation lookaside buffer ("UTLB"), a second translation lookaside buffer ("DTLB"), and a control circuit ("TLB\_CTL") for selecting one of the first and second translation lookaside buffers and performing address translation in accordance with an area of an address space in the virtual address.--

Page 6, lines 8-17:

-- Hereinafter, referring to the accompanying drawings, a description as to a data processor (or information processing system) and the mode of certain aspects of the preferred embodiments of the system will be made. The circuit elements constituting each block of the embodiment preferably are formed on a semiconductor substrate such as single crystal silicon by means of a technique of semiconductor integrated circuit such as well-known CMOS (complementary MOS transistor) and bipolar transistor or the like, though the elements are not particularly limited thereto. Also, the invention preferably may be realized as an intellectual property ("IP") module (either soft IP or hard IP) as all or a portion of the design data for forming a semiconductor integrated circuit. The IP module preferably is stored in an information-recording medium, and preferably may be subjected to a trade and/or transfer via a telecommunication line, data network or the like.--